Appendix. Design example: The DP32 microprocessor

Throughout this thesis we use design descriptions from a hypothetical processor called the DP32 as running example. These descriptions are taken from the first edition of *"The VHDL Cookbook"* by Peter J. Ashenden of University of Adelaide, South Australia* [Ashenden 90]. The DP32 is a hypothetical 32-bit micro-processor with a simple instruction set. There are 256 general purpose registers, a program counter and a condition code register. The memory accessible to the DP32 consists of 32-bit words, addressed by a 32-bit word address. Tables 15-16 list the instruction set of the processor. Figure 31 shows its port diagram.

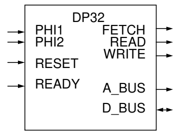

Figure 31. *DP32 port diagram*

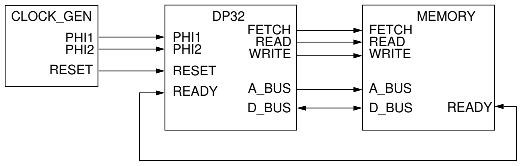

Figure 32. *Test bench circuit for the DP32 microprocessor. The clock_gen component generates the two-phase clock and reset signal to drive the processor. The memory stores a test program and data. These behavioural models for these two components are connected in the structural description of the test bench.*

*. Mr. Ashenden kindly gave permission to use his microprocessor design in this thesis.

The actual microprocessor is embedded in a test bench circuit which is depicted in Figure 32. As this thesis is about CAD frameworks and not about electronic design, the detailed design description is not relevant to us. Examples taken from this description are used throughout the text to illustrate concepts. What is relevant, however, is the overall disposition of the design. Figure 33 depicts the composition hierarchy of the design description for the DP32 test bench circuit along with two configurations.

Instruction	Name	Function
Br-ivnz	branch	if cond then $PC \leftarrow PC + disp32$
Brq-ivnz	branch quick	if cond then $PC \leftarrow PC + i8$
Bi-ivnz	branch indexed	if cond then $PC \leftarrow r1 + disp32$
Biq-ivnz	branch indexed quick	if cond then $PC \leftarrow r1 + i8$

Table 15. *DP32 branch instructions*

Instruction	Name	Function
Ld	load	$r3 \leftarrow M[r1 + disp32]$
St	store	$M[r1 + disp32] \leftarrow r3$
Ldq	load quick	$r3 \leftarrow M[r1 + i8]$
Stq	store quick	$M[r1 + i8] \leftarrow r3$

Table 16. *DP32 load and store instructions*

Instruction	Name	Function
Add	add	$r3 \leftarrow r1 + r2$
Sub	subtract	$r3 \leftarrow r1 - r2$
Mul	multiply	$r3 \leftarrow r1 \times r2$
Div	divide	$r3 \leftarrow r1 \div r2$
Addq	add quick	$r3 \leftarrow r1 + i8$
Subq	subtract quick	$r3 \leftarrow r1 - i8$
Mulq	multiply quick	$r3 \leftarrow r1 \times i8$
Divq	divide quick	$r3 \leftarrow r1 \div i8$
Land	logical and	$r3 \leftarrow r1 \wedge r2$
Lor	logical or	$r3 \leftarrow r1 \vee r2$
Lxor	logical exclusive or	$r3 \leftarrow r1 \oplus r2$
Lmask	logical mask	$r3 \leftarrow r1 \wedge \neg r2$

Table 17. *DP32 arithmetic and logic instructions*

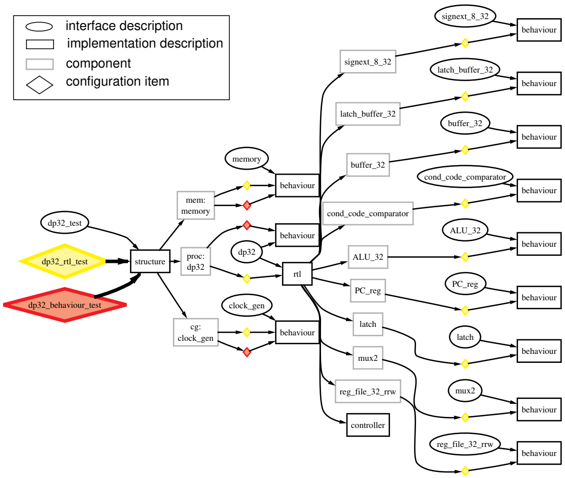

Figure 33. *Structure of the design description for the DP32 test bench circuit. Two design configurations are shown. One, in which a behavioural description of the microprocessor is used; the other one which uses a structural description.*